SUCHARITH S. DEVARAM

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Education

California State University, Fresno (Fresno State), Fresno, CA — expected 05/2026
M.S., Electrical and Computer Engineering — CGPA: 3.0/4.0

Relevant coursework: VLSI circuits and systems, Semiconductor device manufacturing, Digital system testing and testable design, Fundamentals of SEM, Design Optimization for Engineering Systems

Kakatiya Institute of Technology and Science (KITS), Warangal, India — 05/2024
B.Tech., Electronic and Communication Engineering — CGPA: 8.15/10

Relevant coursework: VLSI, Non-Linear Control Systems AIML using Python, VHDL, Digital Design and Digital Signal Processing, Embedded Systems, Industrial Internet of Things (IIoT), Cellular and Mobile Communication

Skills

Electrical Engineering: Electrical schematics, system-level testing, fault analysis, troubleshooting, technical documentation, Scanning Electron Microscopy, Tektronix 4200A-CVIV parameter analyzer
Software & Tools: MATLAB, Simulink, Verilog HDL, ModelSim, Synopsys Design Compiler, TetraMAX, Cadence Virtuoso, Innovus, Microsoft Office

Engineering Project Experience

Multi-Arm Robotic Harvest Optimization, Fresno, CA — 8/2025-12/2025

- Designed a MATLAB-based optimization model to coordinate three robotic arms for automated harvesting
- Minimized total travel distance using linear programming transportation methods (VAM–MODI)
- Performed runtime and performance analysis confirming real-time feasibility

Documented system assumptions, constraints, and results in a formal engineering report

Electrical System Design & Testing -Shift Register Module, Fresno, CA — 1/2025-5/2025

- Designed an 8-bit SIPO shift register which underwent functional simulation, RTL-to-gate level synthesis, DFT scan insertion and test pattern generation.
- Analyzed circuit's area, power and timing reports and test coverage using Synopsys tools and understood how fault insertion and DFT is implemented in complex circuits.
- Scan insertion was implemented using a Design compiler using TCL-based flow to enhance testability and Automatic test pattern generation was performed using Synopsys Tetarmax.
- 98.72% test coverage for the design with 154/160 faults being detected and generated schematic representation of the same design.

Low-Power and Fault-Tolerant D FF Design, Fresno, CA — 1/2025-5/2025

- Developed a low-power, fault-tolerant D Flip-Flop (DFF) architecture by integrating a Modified Self-Voltage Level (SVL) technique for leakage reduction and parity logic for real-time error detection and correction.
- The design targeted power optimization during standby states and ensured single-bit error resilience, making it ideal for sub-45nm VLSI systems. Functional simulation was performed in ModelSim, synthesis and power analysis in Synopsys Design Compiler, and analog-level validation in Cadence Virtuoso.
- Results confirmed significant leakage reduction and reliable error monitoring, suitable for high-dependability, energy-efficient digital systems.

Comparative Analysis of Plasma Assisted Au-Pd Cu sputter Coatings, Fresno, CA — 1/2025-5/2025

- Part of a 4-member group which investigated the deposition of both copper and gold-palladium coatings on top of an implanted silicon substrate which were sputtered using magnetron sputtering methods.
- Scanning electron microscopy was used to analyze the surface, structure, and coating thickness, and gained insights into the performance and quality of Cu and Au-Pd coatings produced by these methods.
- Especially focused on analysis of electrical properties of the samples by calculating the impedance, resistance and capacitance of the samples using Impedance analyzer.

Leadership/Experience

Supplement Instructor,
California State University, Learning Center, Fresno, CA 01/2025-Present

- Supplemental Instruction leader for ECE 90, Principles of electrical circuits, assisting students in understanding the concepts of ECE 90 through various activities, performing duties like creating planning forms, content, arranging sessions that students can utilize as an extra help.

Treasurer,
KITS Electronics and Communication Engineering Association (ECEA), Warangal, India 8/2023-5/2024

- Headed 20+ association events, managed finances ~$2,400 during Sumshodhini Technical Symposium (Feb 2-3, 2024)

Joint Secretary,
KITS Literary and Extramural Club, Warangal, India 8/2023-5/2024

- Organized and acted as Head of the Organization committee of KITS MUN (March 22, 23&24 2024)

Student Organizer,
KITS Springer International Conference on Computers and Communications Tech 2023(IC3T), Warangal, India 10/2023

- Scheduled and managed meetings with presenters and introduced conference panelists and anchored the inauguration and valedictory program